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Claims

[c1] What is claimed is:

1.A method for fabricating a trench capacitor, comprising:

providing a substrate having a deep trench etched therein;

doping the deep trench to form a buried plate electrode in the substrate adjacent to a lower portion of the deep trench;

forming a node dielectric layer on interior surface of the deep trench;

depositing a first conductive layer in the deep trench;

recessing the first conductive layer to a first depth in the deep trench;

forming a collar oxide layer on sidewall of the deep trench above the first conductive layer;

depositing a second conductive layer on the first conductive layer and the collar oxide layer;

recessing the second conductive layer to a second depth inside the deep trench;

forming a pair of symmetric spacers on sidewall of the deep trench above the second conductive layer in a first direction and exposing a silicon sidewall of the deep

trench above the second conductive layer in a second direction, wherein the first direction is substantially orthogonal to the second direction;
depositing a third conductive layer on the second conductive layer and on the spacers; and
recessing the third conductive layer to a third depth inside the deep trench.

[c2] 2.The method of claim 1 wherein after recessing the third conductive layer to a third depth inside the deep trench, the method further comprises the following step: out diffusing dopants of the second conductive layer to the silicon sidewall in the second direction via the third conductive layer, thereby forming a buried strap out diffusion region that is used to electrically connect the deep trench capacitor with a source region of an access transistor, wherein out diffusion of the dopants of the second conductive layer in the first direction is blocked by the spacers.

[c3] 3.The method of claim 1 wherein the method of forming a pair of symmetric spacers on sidewall of the deep trench above the second conductive layer in a first direction comprises the following steps:
depositing a thin dielectric layer on sidewall of the deep trench and on the second conductive layer;
depositing a thin amorphous silicon layer on the thin di-

electric layer;

performing a tilt angle ion implantation process to selectively and symmetrically implant P type ions into the thin amorphous silicon layer on the sidewall of the deep trench in the first direction;

anisotropic etching the thin amorphous silicon layer and the thin dielectric layer, thereby exposing the second conductive layer;

selectively etching the thin amorphous silicon layer that is not ion implanted with the P type ions; and

removing the thin dielectric layer that is not covered by the remaining thin amorphous silicon layer, thereby forming the symmetric spacers and exposing the silicon sidewall.

[c4] 4.The method of claim 3 wherein the P type ions are BF_2 ions.

[c5] 5.The method of claim 3 wherein the method of selectively etching the thin amorphous silicon layer that is not ion implanted with the P type ions comprises the use of diluted ammonia solution.

[c6] 6.The method of claim 3 wherein the thin dielectric layer is a CVD silicon oxide layer.

[c7] 7.The method of claim 3 wherein the thin dielectric layer

has a thickness of about 100~200 angstroms.

[c8] 8.The method of claim 3 wherein the thin amorphous silicon layer has a thickness of about 50 angstroms.

[c9] 9.The method of claim 1 wherein the first conductive layer is made of polysilicon.

[c10] 10.The method of claim 1 wherein the second conductive layer is made of polysilicon.

[c11] 11.The method of claim 1 wherein the third conductive layer is made of polysilicon.